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THESIS

A DIRECT SEQUENCE - CODE DIVISION MULTIPLE ACCESS/BINARY PHASE SHIFT KEYING (DS-CDMA/BPSK) MODEM DESIGN

by

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March 1997

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13. ABSTRACT *(maximum 200 words)*

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The hardware used in the functional realization of a working design is also discussed, the preliminary operational characteristics of a spread spectrum BPSK modem are achieved. The multi-user performance analysis is conducted using Bit Error Rate (BER) test equipment (HP1645A). The development of the final version of the modem operating at radio frequency (RF) is not conducted, but proof of concept is provided.

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A DIRECT SEQUENCE - CODE DIVISION MULTIPLE ACCESS/ BINARY PHASE SHIFT KEYING (DS-CDMA/BPSK) MODEM DESIGN

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requirements for the degree of

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I. INTRODUCTION

Due to the increasing demand on capacity and privacy, code division multiple access (CDMA) is a very attractive area for research and development in cellular radio systems.

Spread spectrum systems utilize a high chip rate coding sequence to spread and despread the information data. By the use of a pseudo-noise (PN) sequence, the baseband information spectrum is spread to wideband spectrum. The spread-spectrum signal usually has a power spectral density below the channel noise level. When two spread spectrum signals are sharing the same frequency band, there is a certain amount of crosstalk, or mutual interference. The interference is negligible since it is possible to design spreading sequences (like Gold sequences) with low cross-correlation values so that the various code sequences are nearly orthogonal. Since system performance degrades as the number of users increase, the number of users in the same frequency band has an upper limit.

The objective of this thesis is to design and build a direct sequence - code division multiple access/binary phase-shift keying (DS-CDMA/BPSK) spread spectrum modem that can be used in a multi-access environment and to test the multi-user performance. The following initial parameters are provided as guidance in formulating the design:

1. BPSK modulation with coherent detection.
2. Direct sequence spread spectrum using Gold Sequences of 31 chips generated from a preferred-pair of m-sequences.
3. Each data bit is spread by one complete Gold sequence. This both simplifies acquisition and improves performance.
4. Data bit rate equal to 1200 bits per second.
5. A maximum number of users of four.

The basic characteristics of direct sequence BPSK system was taken from Dixon [Ref. 1]. For CDMA, the Gold codes were selected based on their low cross-correlation properties as explained in Ziemer and Peterson [Ref. 2]. The design of the acquisition and synchronization circuits was taken from Lam [Ref. 3] and Gibson [Ref. 4].

II. DS-CDMA/BPSK MODEM DESIGN AND OPERATION

A. SYSTEM OVERVIEW

The modulator section of the DS-CDMA/BPSK modem design has four main functional blocks:

1. Pseudo-random noise (PN) sequence generator [Ref. 1, 2].
2. Data and clock generator [Ref. 5].
3. Spreader and level shifter [Ref. 6].
4. Low pass filter and mixer [Ref. 7, 8, 9].

The modulator functional block diagram is shown in Figure 1.

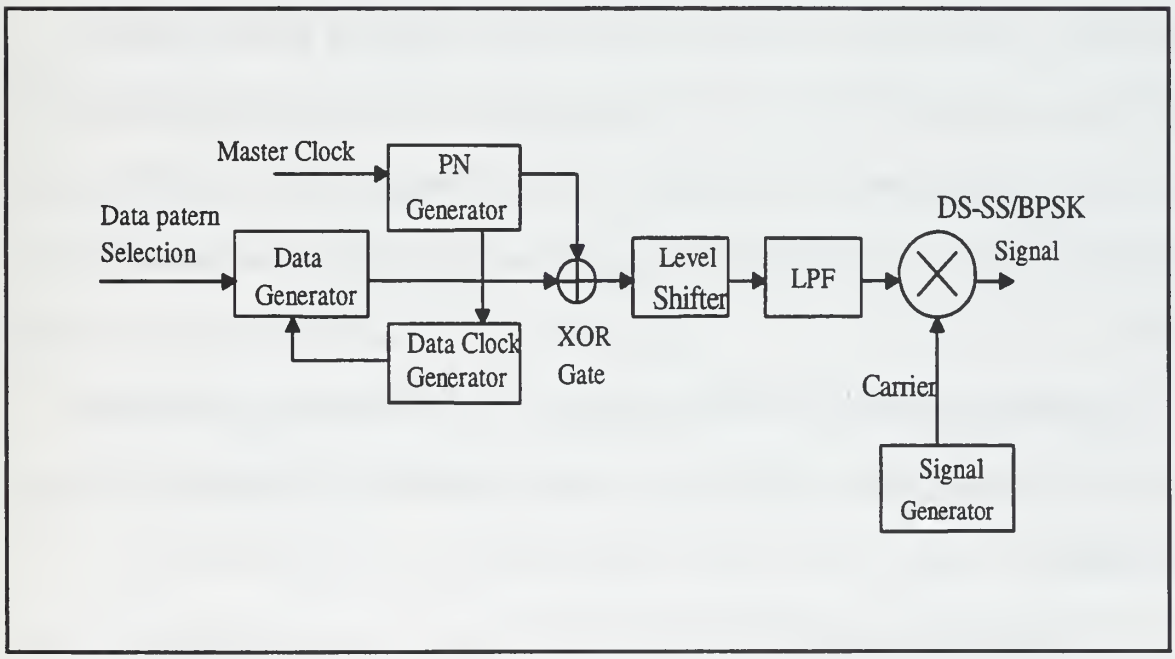

Figure 1. The Modulator Functional Block Diagram

The master clock provides clock pulses for the PN generator and the data generator. The 37.2 kHz master clock is generated by a WAVETEK Model 142 function generator. The PN generator used in the modulation section is driven by the 37.2 kHz master clock.

In this spread spectrum modulator, two 5-bit shift registers are used as a pseudo-random Gold sequence generator. By design, each data bit will contain 31 chips (an entire sequence) of the PN sequence. The spread spectrum modem designed supports a data rate of 1200 bps.

After spreading the data digitally by using an exclusive-or (XOR) gate, the signal levels are shifted from 0 volts and +5 volts to -5 volts and +5 volts, respectively. To suppress the side lobes of the baseband spread spectrum signal, a low pass filter with a cut-off frequency of 37.2 kHz was designed and built. The resultant signal at the output of low-pass filter is mixed with the 76.2 kHz carrier signal. This DS-SS/BPSK signal is sent to the receiver directly via hardwire.

The demodulator functional block diagram is obviously more complicated than that of modulator. There are several functions performed by the demodulator:

1. PN sequence generation [Ref. 1, 2].
2. Acquisition and Synchronization [Ref. 3, 4].
3. Spectrum despreading [Ref. 6].
4. Signal demodulation [Ref. 3, 10, 12, 14].

The demodulator functional block diagram is shown in Figure 2.

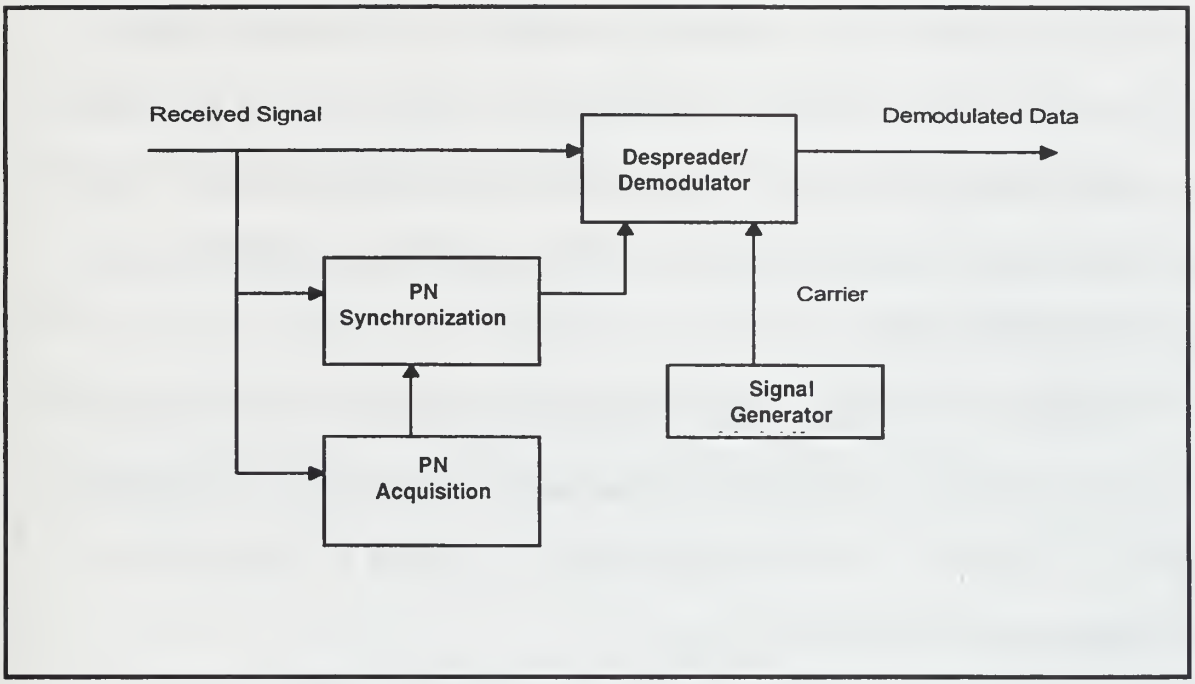

Figure 2. Demodulator Functional Block Diagram [Ref. 3]

After the PN acquisition subsystem has accomplished its function, it generates the PN signal within $\pm T_c / 2$ of the incoming PN signal. To obtain the phase difference in the range of $\pm T_c / 2$, the acquisition subsystem searches through a set of 31 different discrete phases and select the one which yields the highest correlation with the incoming PN signal.

Once the phase of the local PN signal is within $\pm T_c / 2$ of the incoming PN signal, the synchronization circuit attempts to bring the phase difference to zero.

The PN signal from the synchronization circuit and a coherent carrier are used for despreading and demodulation processes to obtain an estimate of the transmitted data.

PN acquisition is performed before synchronization. Since the carrier frequency and phase are available, coherent carrier demodulation is used with

the acquisition circuit. In a real modem application, the carrier phase is unknown and recovered by driving a phase-locked loop (PLL) through a square-law device (full-wave rectifier) [Ref. 4], which is not included in this prototype design. Once the PN code phase has been acquired, the PN synchronization circuit is initiated.

B. PN GENERATOR

The pseudo noise Gold sequence generator consists of a pair of preferred m-sequence generators. A generalized Gold sequence generator block diagram is shown in Figure 3. The PN clock signal in Figure 3 is generated by a WAVETEK Model 142 function generator.

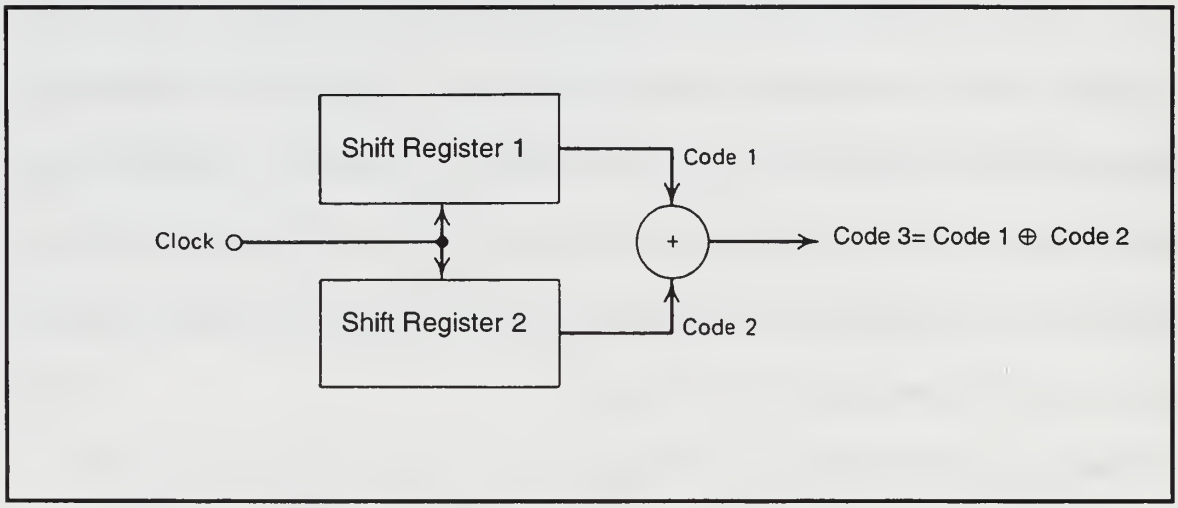

Figure 3. Gold Code Sequence Generator Configuration [Ref. 1]

Each m-sequence generator itself consists of two 4-bit serially connected shift registers (74LS95) and XOR (74LS86) gates [Ref. 6]. The main structure of the PN generator design was taken from Dixon [Ref. 1], although many variations are available from other sources [Ref. 3, 10]. An illustration of the Gold sequence generator is shown in Figure 4.

In the design of the first of the two m-sequence generators, the third and fifth stages of the shift register are modulo-2 added by an XOR gate. The resultant logic level is fed back to the input of the first stage of the shift register.

The resultant PN sequence, which is the output of the fifth stage of the shift register, is a maximal length sequence consisting of a series of high and low logic levels (ones and zeros) in pseudo random order. This binary sequence is repeated every 31 clock cycles and each sequential pattern is identical.

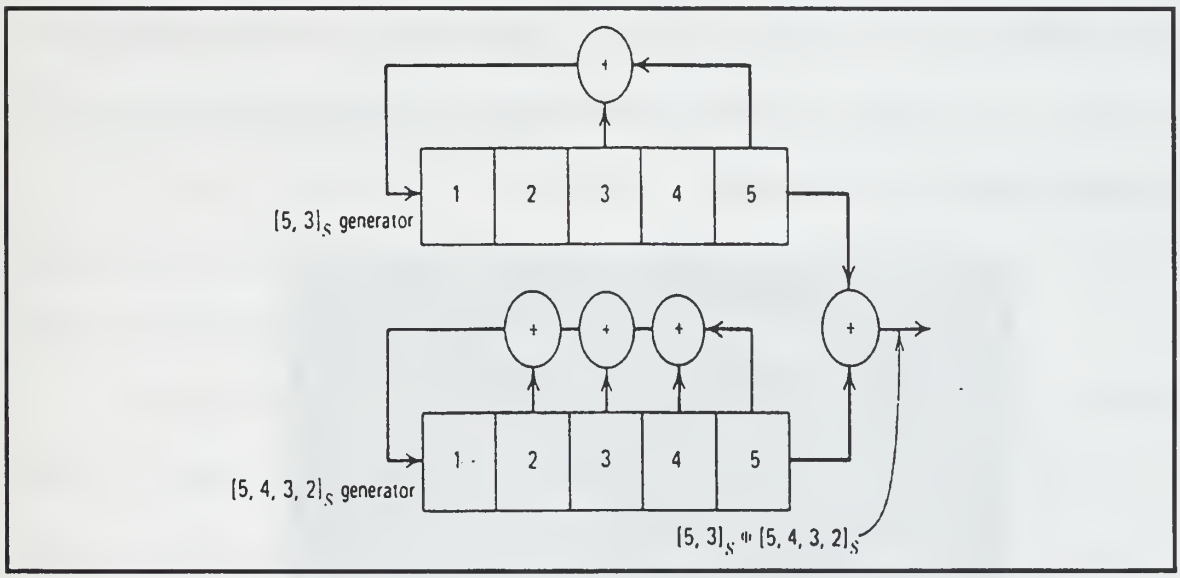

Figure 4. Illustration of the Gold Code Generation

The period of the sequence results from the relationship in Equation 2.1 [Ref. 1];

$$L = 2^m - 1 \tag{2.1}$$

which relates the number of stages in the shift register (m) to the length of the sequence (L), up to the point of repetition. The first Gold sequence is the output of only the first m-sequence generator.

A representative sample of the first Gold sequence employed in spreading and despreading sections is shown in Figure 5. A 31-bit period of the Gold sequence in Figure 5 is marked by the vertical dotted lines.

The generation of the 1.2 kbps data clock is accomplished internally by using the master clock used in the PN generator. To accomplish this, all five outputs of the shift register stages are fed to an AND gate (7430) [Ref. 13] to generate a 1.2 kHz square wave clock which is required for 1.2 kbps data. Thus, this clock is obtained by dividing 37.2 kHz master clock by 31. The AND gate output gives a logic one (+5V) when all five inputs are logic one, which occurs one time in every 31 chips' duration.

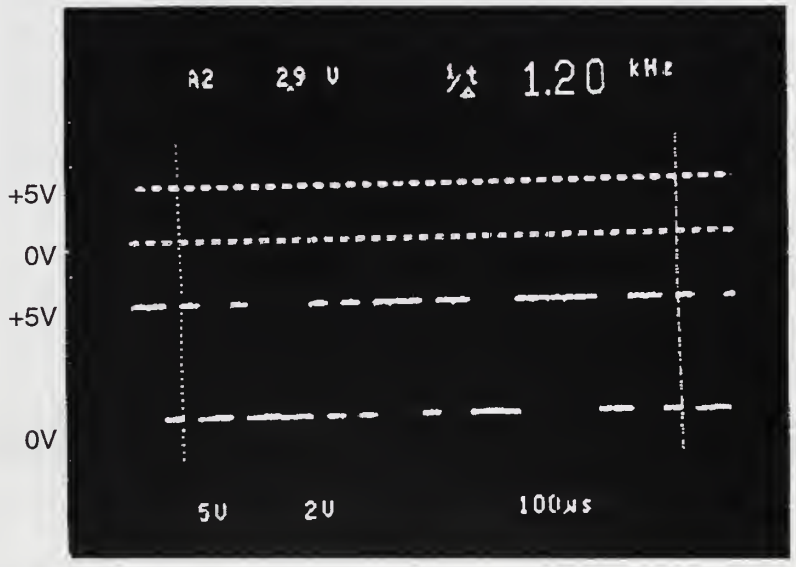

Figure 5. Top: Clock (37.2 kHz)
Bottom: PN Sequence (Gold Sequence)

C. MODULATION

The BPSK signal at the output of the mixer in Figure 1 is generated by the PN encoded data stream and a sinusoidal carrier. The spreading operation for

the BPSK spread spectrum signal in this design occurs in two places. The 1.2 kbps data stream is modulo-2 added to the PN sequence in the modulator section to create the PN encoded data stream. An XOR gate is used for this process, and since the inputs to the XOR gate are TTL voltages with a bipolar characteristic, the function performed by the XOR is essentially a spreading operation. This fact may seem trivial but it creates an important effect as far as the treatment of the signal in the modulation process and its subsequent demodulation process are concerned. The TTL voltages are converted to +5V and -5V for interfacing with the analog components in this design.

The mixer employed for modulation consists of an XOR gate and an internally trimmed, precision IC multiplier (AD534). The AD534 is also commonly known as an analog voltage multiplier [Ref. 11].

The spreading section consists of two elements: the spreading gate and the level shifter. The spreading gate is an XOR gate that modulo-2 adds the 1.2 kbps data signal and the PN sequence with a chip rate of 37.2 kchip per second.

The inputs to the XOR gate are the TTL data stream (at 1.2 kbps) and the PN sequence generated by the PN generator section of the modulator. The output of the XOR gate can be thought of as essentially a bi-phase shifted PN sequence. Considering the length of the sequence (31 chips) as one period, each data transition (which contains 31 chips) causes the PN sequence to invert. The PN sequence phase relationship is thus similar to that of a bi-phase shifted sinusoid since the PN sequence is also a periodic wave form. The maximum

periodicity is the reciprocal of the data rate, 833.33 μs. An alternating data sequence (square wave) creates the maximum number of inversions of the PN sequence. For testing purposes, a 600 Hz square-wave is used to simulate the 1.2 kbps data stream.

The PN output of the XOR is fed to a level shifter. The level shifting is accomplished by connecting the output of the spreading gate to a LM311 voltage comparator [Ref. 13, 15] whose reference voltage is set at 2.5V, the mid-point between 0 and 5V. The resultant output is a balanced PN encoded sequence with bipolar voltages of +5 and -5 volts as the digital logic PN sequence changes the logic levels between 0 and 5 volts.

The resulting PN data stream from the comparator is interfaced with the (AD534) mixer. This signal is connected directly to pin 6 of the mixer (AD534) which corresponds to its Y1 input. The sinusoidal carrier from the signal generator is also connected directly to the mixer on pin 1 which corresponds to the X1 input. The mixer (AD534) accomplishes multiplication according to the following equation [Ref. 11].

$$V_{out} = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10} + Z_2 \qquad (2.2)$$

The wiring configuration for the mixers shown in Appendix B is taken from Reference 11. This reflects a standard multiplication configuration and functions equally well as a mixer.

The mixer translates the frequency by multiplying the spread data and carrier. The output is the carrier frequency changing its phase with the change of phase of the PN sequence.

D. DEMODULATION

A detailed scheme of demodulator is shown in Figure 6. The demodulation process reverses the order in which the PN sequence and the data are modulated with the RF carrier. This is possible since the process of mixing is order-independent. First, the received signal is mixed with the identical PN sequence by using an AD534 multiplier with the same configuration discussed in the modulation section. After the despreading process, the resultant pass-band signal is translated to baseband by mixing it with the carrier signal having the same frequency and the phase as the carrier in the modulator. The frequency translation is achieved by an AD534 multiplier. A fourth order low pass filter [Ref. 15] with a cut-off frequency of 1.2 kHz suppresses the image frequencies after the mixing process. The frequency response of the low pass filter is shown in Figure 7.

The amplification factor of 0.1 of all the mixers employed in the demodulation process is compensated by a non-inverting voltage amplifier (LM318) [Ref. 15]. When the repeating test sequence of "1 0 0 0" is trasmitted, the integrator output in the demodulator is shown in Figure 8 (Bottom). Since an inverting amplifier (LM 318) is employed at the output of the integrator, the bottom trace in Figure 8 has an inverted version of the data, "0 1 1 1".

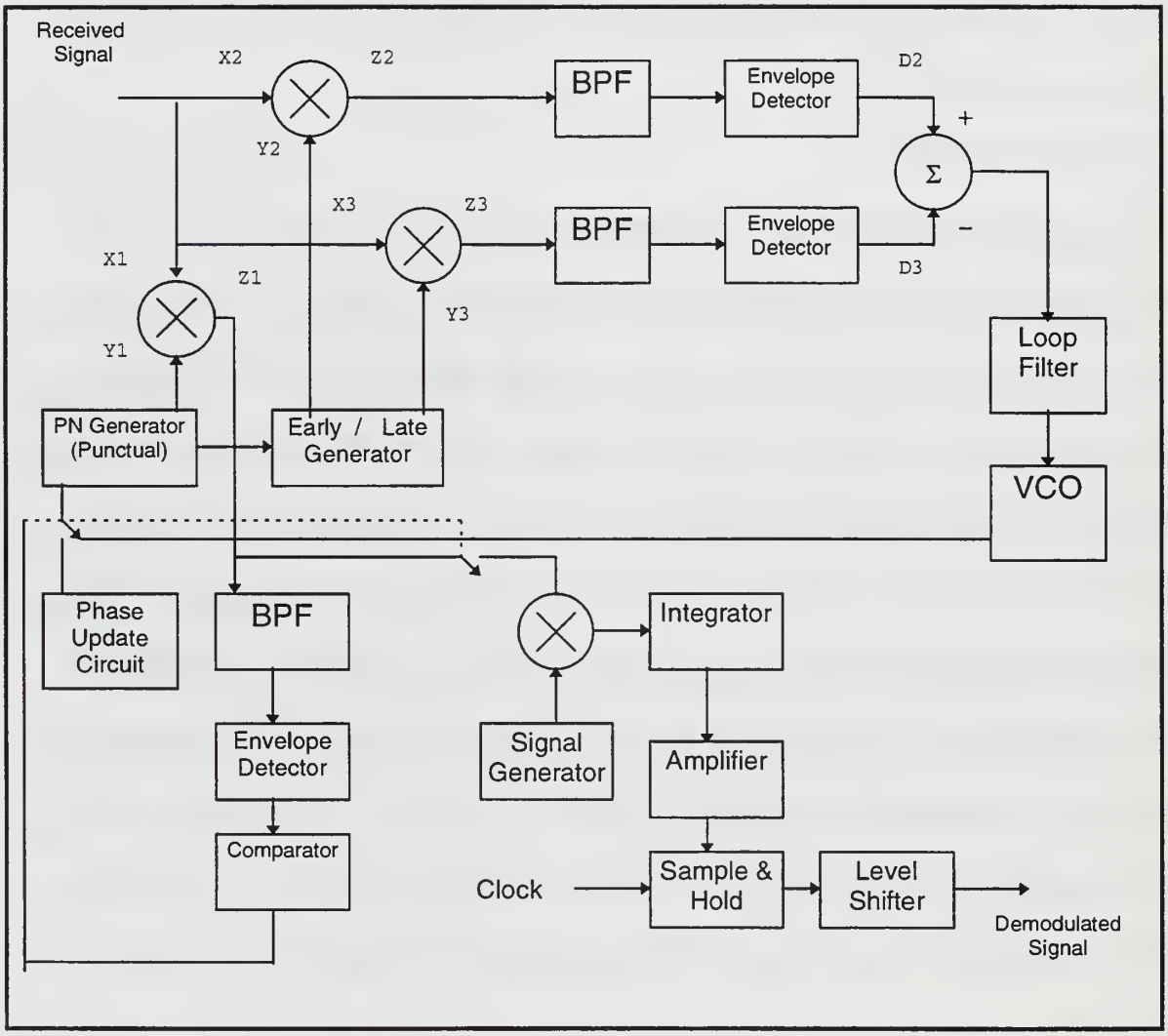

Figure 6. The Functional Block Diagram of the Demodulator

The resultant signal is sampled with 1.2 kHz clock by a sample-and-hold source (LF398) [Ref. 13] and is then applied to a level shifter circuit (LM311).

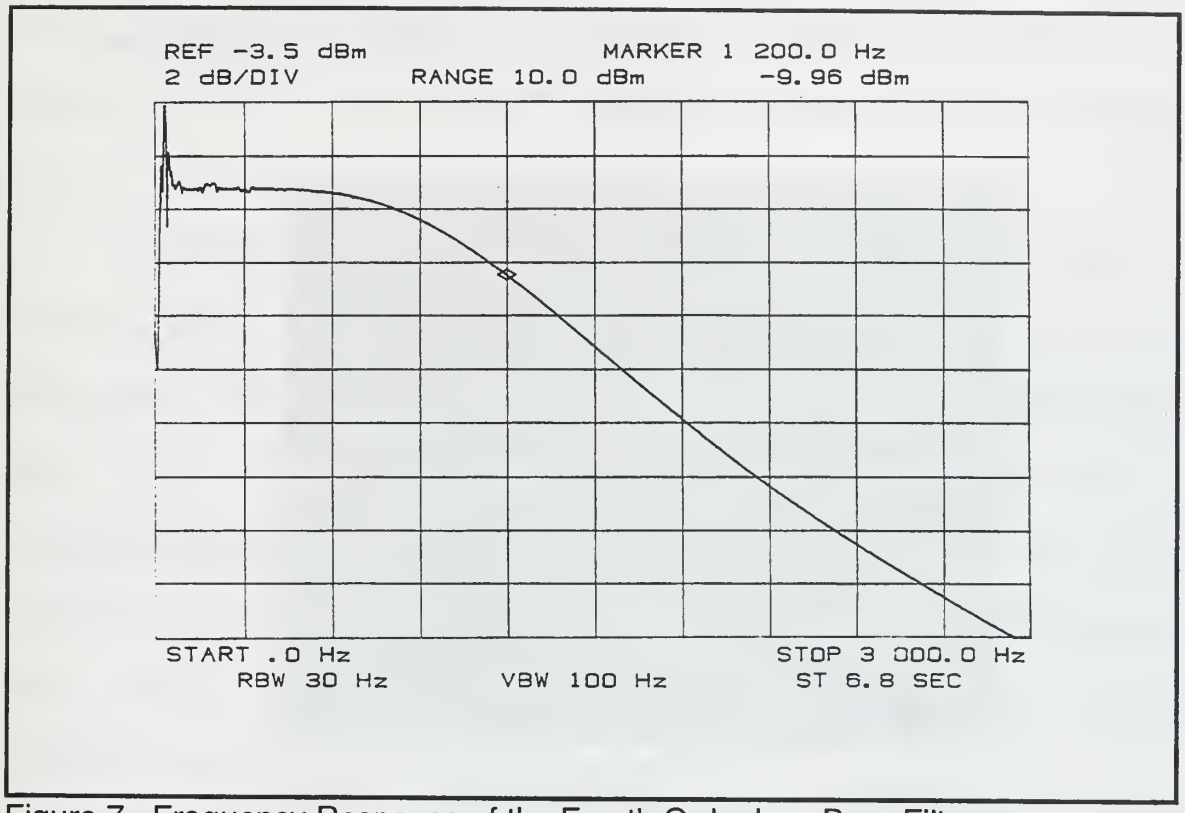

Figure 7. Frequency Response of the Fourth Order Low Pass Filter

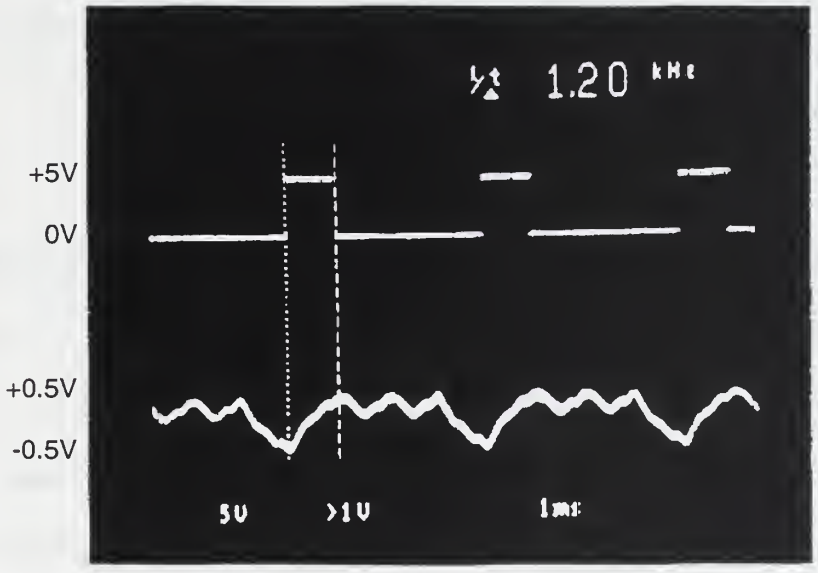

Figure 8. Top: Transmitted Data
Bottom: Integrator Output in the Demodulator

The transmitted information signal and the received signal are shown in Figure 9.

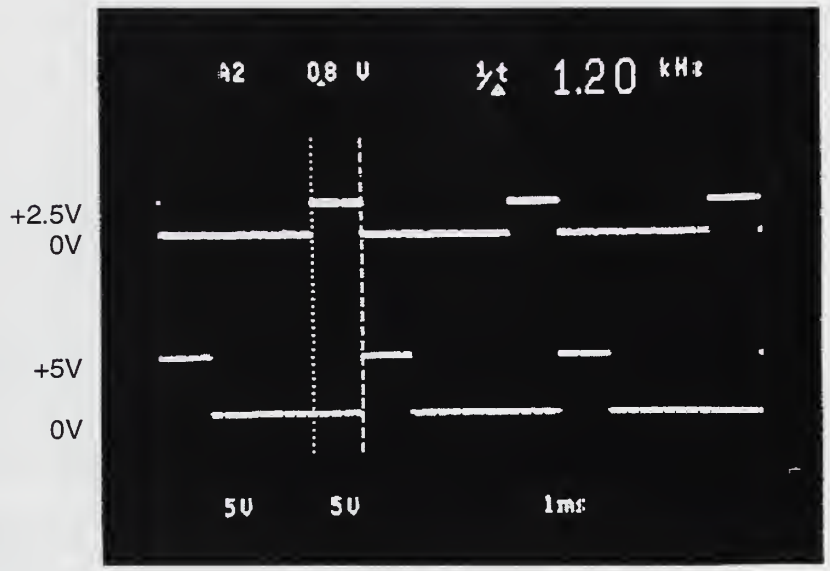

Figure 9. Top: Transmitted Information Signal
Bottom: Received Information Signal

The other two functions performed by the receiver are acquisition and tracking, which are explained in the following sections in detail.

E. ACQUISITION

The acquisition phase of signal demodulation utilizes a sliding correlator. The flow diagram for the sliding correlator is shown in Figure 10, and the implementation of its acquisition phase is shown in Figure 11 [Ref. 1].

There are three digital PN sequences generated in the receiver: early, late, and punctual PN sequences. Punctual refers to the PN sequence (Y1 in Figure 6) which despreads the received signal. Early refers to the PN sequence (Y3 in Figure 6) which is advanced by one-half a chip ahead of the punctual (despreading) PN sequence in time, and late refers to the PN sequence (Y3 in

Figure 6) which is delayed by one-half of a chip behind the punctual PN sequence in time. The punctual PN sequence is employed in the acquisition phase.

As the punctual PN sequence generated in the receiver slides through the incoming signal, variations in the demodulated envelope are sent to a comparator. When correlation occurs, the envelope detector output voltage rises. The threshold voltage on the LM311 employed to mark the point of punctual correlation is set to change the comparator output from low to high when the output of the punctual channel envelope detector goes sufficiently high. This is accomplished by using an analog switch triggered by the punctual correlation signal itself via the LM311 comparator.

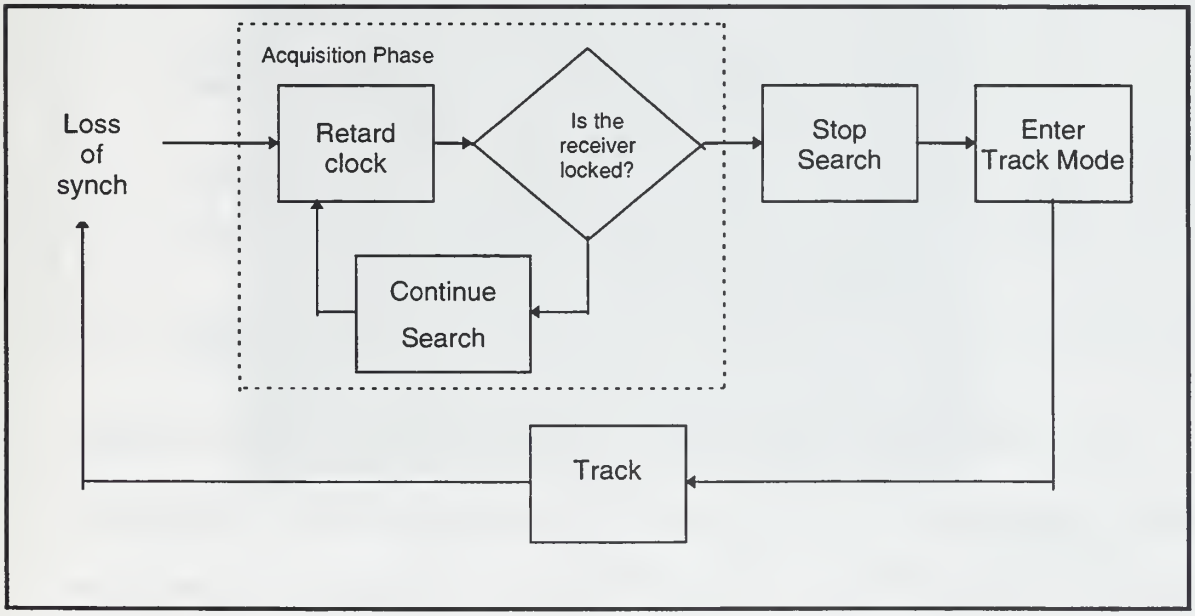

Figure 10. Flow Diagram for Sliding Correlator

The incoming signal is applied to the X1 input of an AD534 analog multiplier while the PN sequence is applied to the Y1 input as shown in Figure

11. While the spread spectrum signal is present at the input of the demodulator, the instantaneous output of the despreader (Z1 in Figure 11) is one of the following two cases. In the first case, the output from the despreader is a BPSK modulated signal where the phase changes are the result of the data transitions only since the PN sequence lines up chip for chip with that of the PN sequence in the spreading process. The second case is a BPSK modulated signal in which the phase changes are the result of two identical but out of phase PN sequences. The misalignment of the PN sequences causes further spreading of the already widened frequency spectrum.

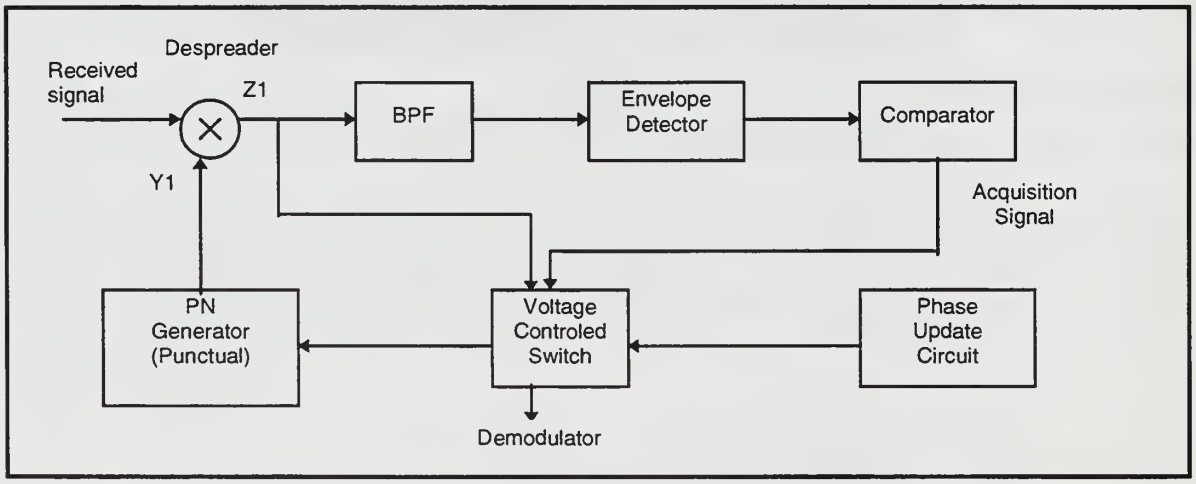

Figure 11. The Block Diagram of the Acquisition Circuit

The output of the despreader is connected to an envelope detector through a band pass filter. The design of the envelope detector is taken from Haykin [Ref. 16]; but unlike the envelope detectors for amplitude modulation, the charging and discharging time constant RC is relatively short compared to the symbol duration. The decision as to whether the received and receiver PN

codes are aligned or misaligned is determined by the voltage level at the envelope detector output.

In the uncorrelated case, the resulting signal at the output of the band pass filter is shown in Figure 11 (Bottom), where the misalignment is one chip (which is greater than $T_c/2$). When the incoming PN sequence is not aligned with the local PN sequence, the envelope detector output is rather low (approximately 0.1V). In this first case, the resulting signal wave form in Figure 12 (Bottom) is representative of each location along the PN sequence in which the alignment difference is one chip (greater than half chip). The vertical dotted lines show the misallignment (26.5μsec) between PN codes in modulator and demodulator.

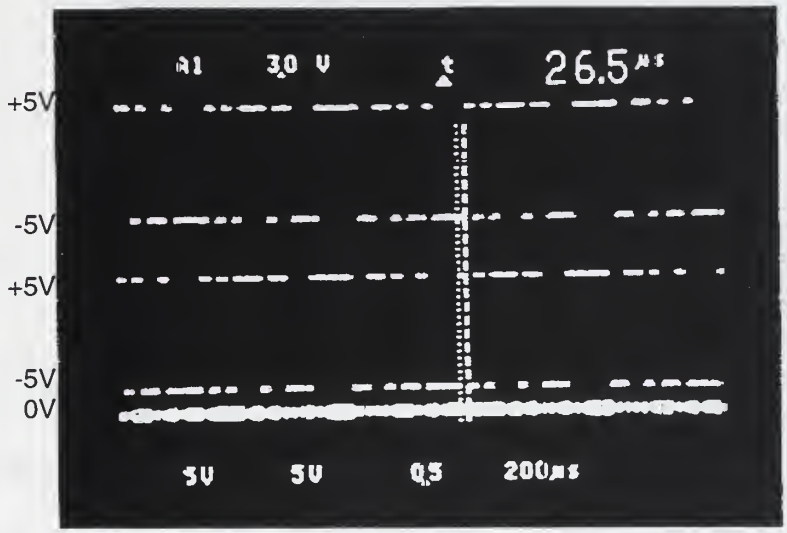

Figure 12. Top: PN sequence Used in Modulation
Middle: Punctual PN Sequence from Demodulator
Bottom: Uncorrelated Output from Band Pass Filter

In the correlated case, the output of the envelope detector is higher and ranges between 1.9V and 2.2V. This higher output is used as an indication of acquisition of the incoming signal and serves to trigger the change from

acquisition to synchronization mode. The output of the band pass filter in the correlated case is demonstrated in Figure 13. The output from the envelope detector is notably greater than the one in the uncorrelated case when the two PN sequences are correlated. This higher output is an indication of the allignment of the PN codes within T_c. Consequently, there is a band of correlation that exists within one half chip either early or late relative to the punctual sequence. Alignment of PN sequences employed in modulator and demodulator can be shown to occur in this region. The demodulation of the received signal starts after the PN code has been acquired.

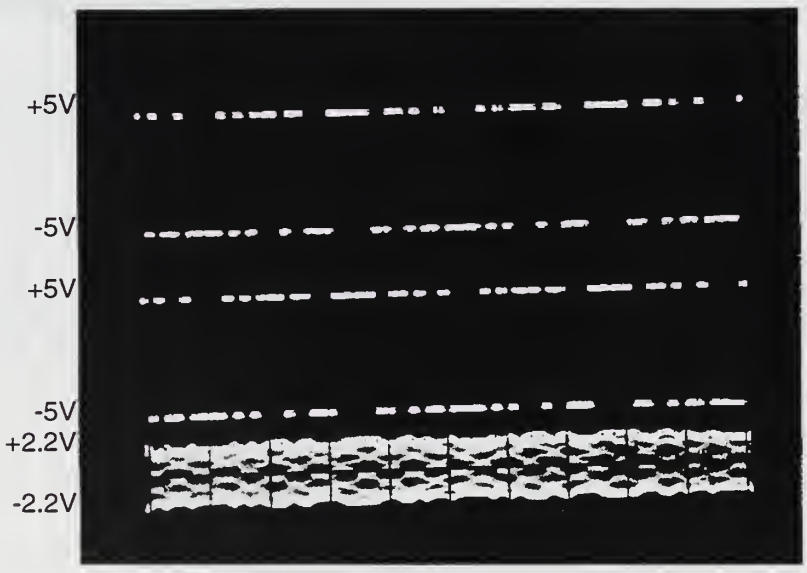

Figure 13. Top: PN Sequence Used in Modulation
Middle: Punctual PN Sequence from Demodulator
Bottom: Correlated Output from Band-Pass Filter

A difference in the correlated versus uncorrelated signals at the output of the envelope detector can also be seen in the analysis of the spectral outputs of the band-pass filter for each case. The uncorrelated and correlated spectra from

the output of the band pass filter of the punctual channel as they appear on a spectrum analyzer are shown in Figures 14 and 15, respectively.

Note that the side lobes of the spread spectrum signal are missing in the uncorrelated output of the band pass filter since they are attenuated by the high Q of the filter. Conversely, when correlation occurs the output spectrum of the band pass filter changes significantly.

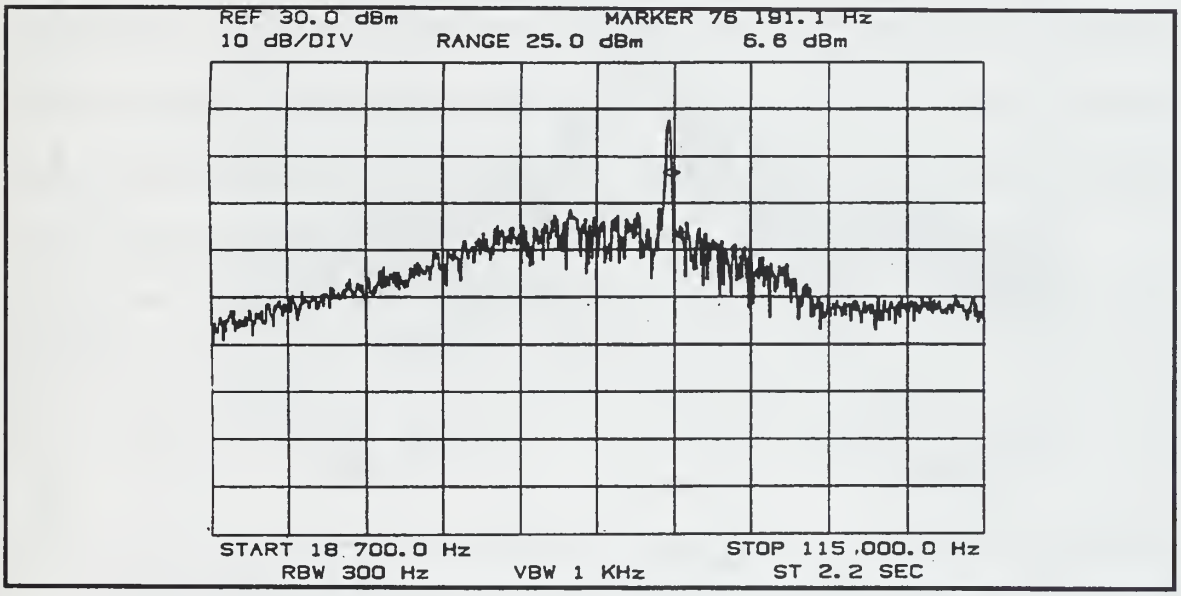

Figure 14. Uncorrelated Spectrum Output of the Punctual Channel Band Pass Filter (The marker shows the carrier frequency f_c=76.2kHz.)

The side lobes that appear at the output of the band pass filter during correlation are representative of the despread BPSK modulated carrier. In fact, the spectral distance between the center frequency of the main lobe and the side lobes in the correlated case is approximately one and one half times the data rate (R_b).

Thus, the data may be recovered from the correlated signal since the indication that the sequence is correlated comes directly from the output of the band pass filter.

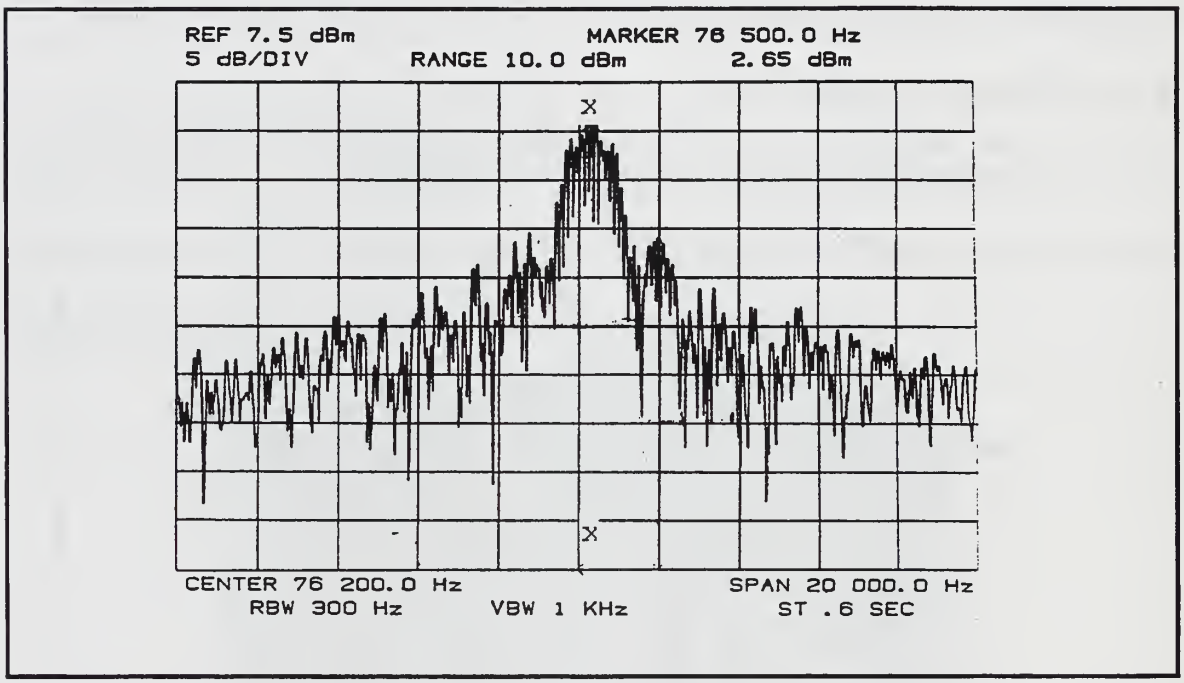

Figure 15. Correlated Spectrum Output of the Punctual Channel Band Pass Filter (The marker x shows the carrier frequency f_c=76.2kHz.)

F. SYNCHRONIZATION

The synchronization circuit consists of a loop that monitors the error and adjusts the desired signal in such a way so that the error goes to zero. The tracking is initiated after the acquisition circuit has brought the phase difference between the incoming and the local PN signals to within one chip duration (T_c). The primary concern in an operational spread spectrum system is to ensure that

the demodulator can despread the incoming spread spectrum signal to a narrow band signal from which the original transmitted data may be recovered.

To accomplish this, a demodulation design must possess two critical features. First, the same PN sequence must be used in the demodulation process as was used to originally encode the data in the modulation process. Second, the frequency at which the demodulation PN generator is clocked must be controlled and compensated for differences between it and the PN sequence imbedded within the incoming signal. This design uses a means of frequency control which takes the form of a delay lock loop. The block diagram of the delay lock loop with half chip delayed is shown in Figure 16 [Ref. 1].

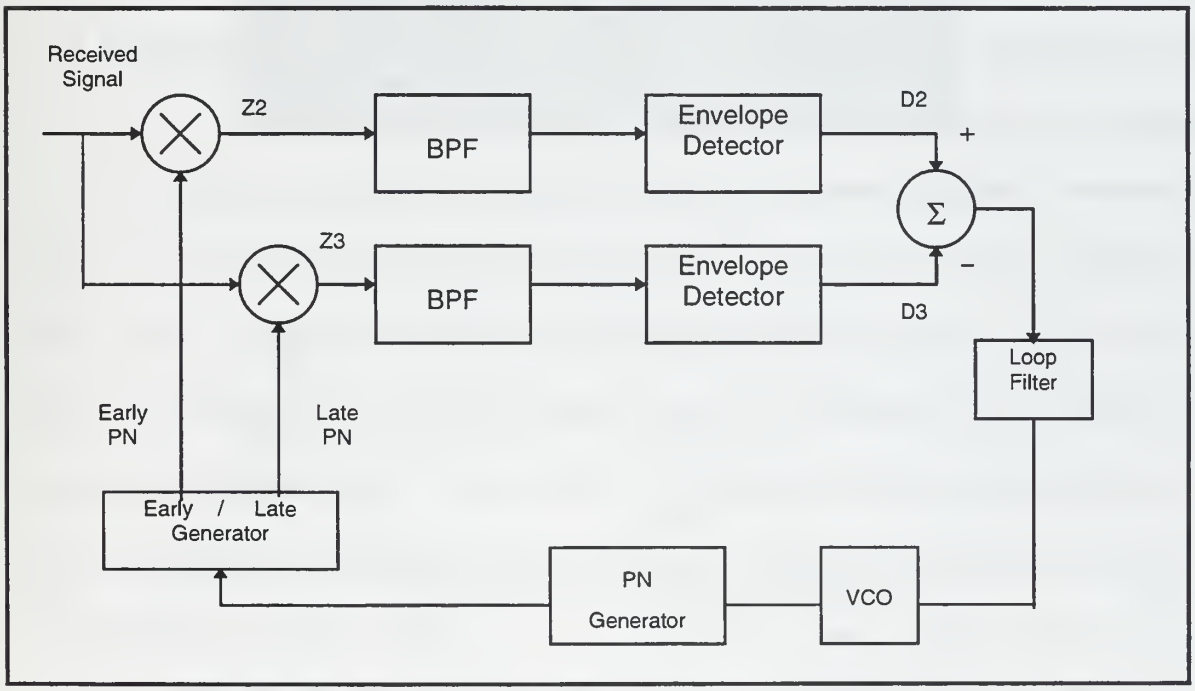

Figure 16. Delay Lock-Loop with Half-Chip-Delayed Correlator [Ref. 1]

The mixer outputs Z2 and Z3 are fed through band pass filters of identical configurations to that used in the punctual channel (Figure 6). The early and late

channel filter outputs are each connected to envelope detectors. The envelope detector outputs are used in the tracking of the incoming signal. These early and late correlation signals can clearly be seen as maximum when each of the respective PN sequences is in correlation with the incoming signal. As any one of the PN sequences begins to come within $\pm T_c$ of the incoming signal, the output of the associated envelope detector begins to rise linearly from the uncorrelated output value to the maximum value achieved when the PN sequences are exactly correlated. Beyond the maximum value, as the PN sequences pass one another, the envelope detector output falls to the value corresponding to that of an uncorrelated signal. This triangular pulse is known as the correlation triangle. Figure 17 shows the ideal correlation triangle as a function of the amount of synchronization error τ [Ref. 4].

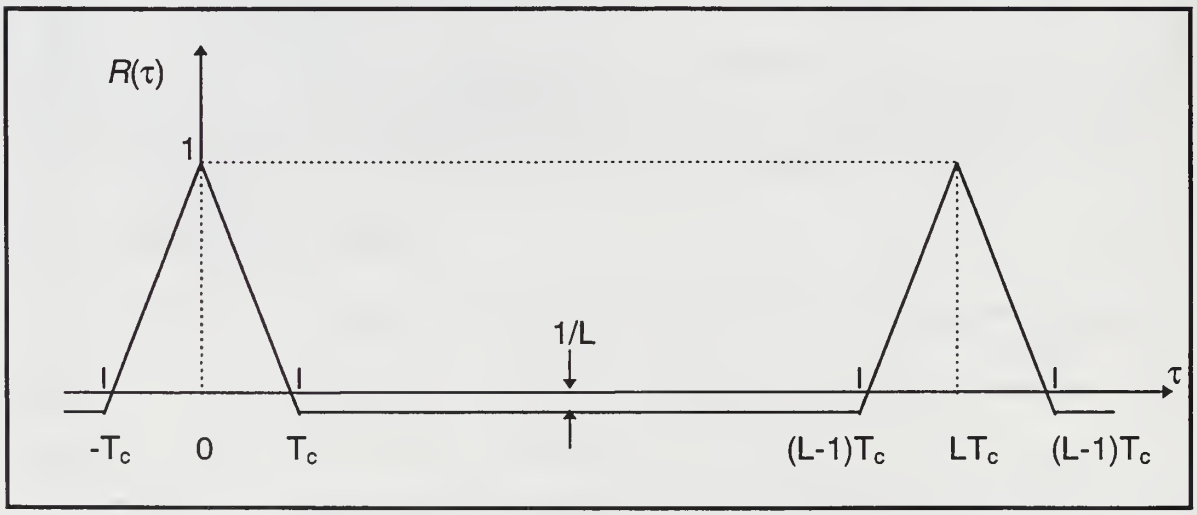

Figure 17. Ideal Correlation Triangle [Ref. 4]

The early-late channel envelope detector outputs are shown in Figure 18.

The timing delays used to establish the early and late PN sequences allow for the creation of a linear voltage control zone for use in feedback control. The voltage generated by the early minus late circuitry during operation in track mode is applied to VCO through the loop filter. The outputs of the early and late

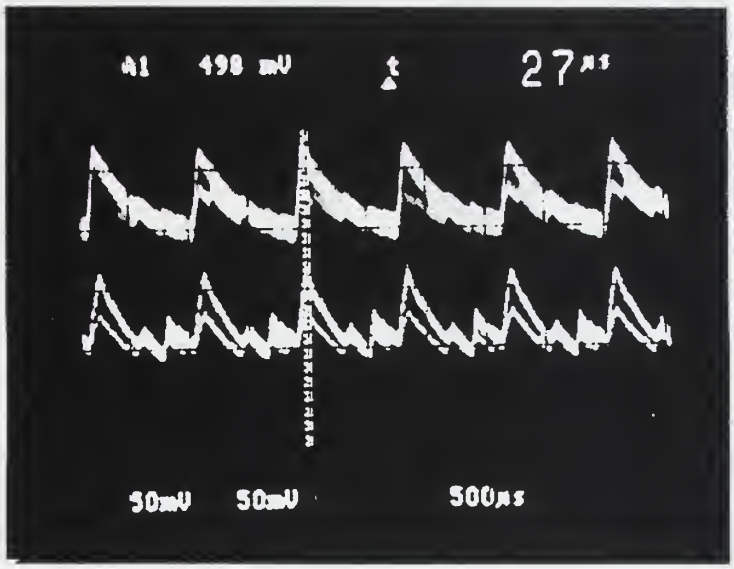

Figure 18. Early-Late channel Envelope Detector Outputs

envelope detectors (D2 and D3 in Figures 6 and 16) are amplified using standard non-inverting amplifier configurations employing LM318 operational amplifiers [Ref. 6]. The output of the late correlation signal is then inverted and added to the early correlation signal, thus creating an early-late correlation triangle pair. The ideal early-late correlation signal is shown in Figure 19. In order for this feedback voltage to be useful in any spread spectrum design, the punctual signal must be within one half chip of maximum correlation. The circuit diagram for the feedback control section is shown in Appendix B as part of Figure B-4.

When a frequency difference exists, the punctual PN sequence will attempt to drift (early or late) out of correlation if a correcting voltage is not applied to the VCO. Upon drifting from the maximum correlation value, the early or late correlation signal (depending upon the direction of drift) will correspondingly add to or subtract from the control voltage sensed by the VCO.

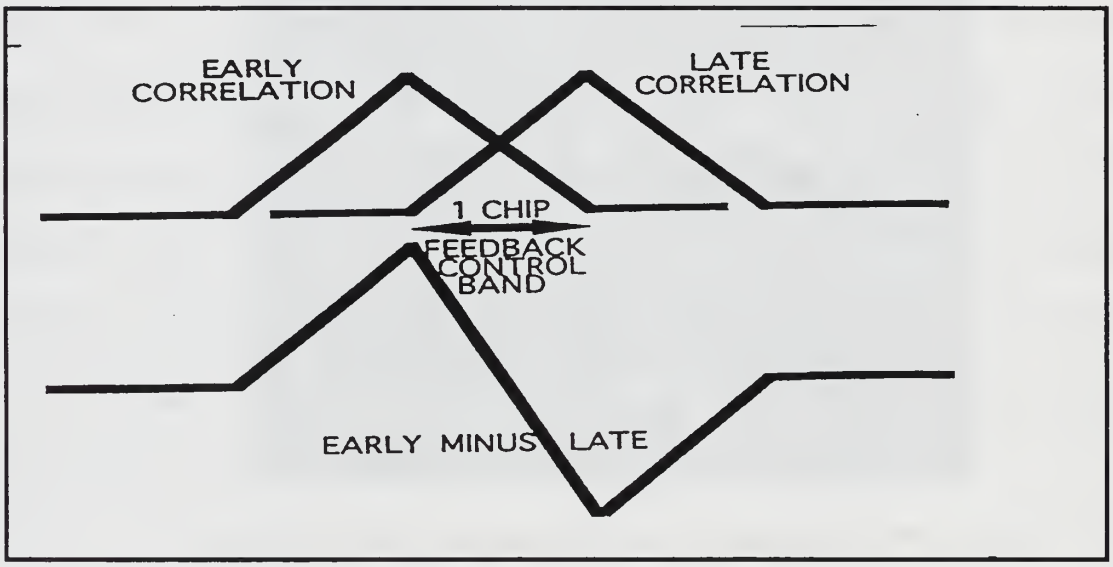

Figure 19. Ideal Early Minus Late Correlation Signal

The VCO will then adjust the frequency of oscillation until the frequency that matches the maximum point of correlation is reached. This feedback continues throughout the receipt of the incoming signal, and the demodulator is thus maintained in a tracking mode and may further translate the incoming signal back into the data bits that were transmitted.

G. BAND PASS FILTERS

The band pass filters in the acquisition and synchronization circuits are identical and provide sufficient filtering to help eliminate noise that may interfere with the proper demodulation of the incoming signal.

Cost and component availability are also concerns. The design of the filters here dictates an active filter realization using operational amplifiers [Ref. 7, 8, 9]. Although a majority of the power consumed in this design is attributed to the operational amplifiers that make up the band pass filters, aspects of this solution may be viable for ground station applications where the power consumption of the modem is not a concern. Passive elements such as crystal filters can be used in a final design if desired. The characteristics of the design remain the same and, as a matter of practicality, the use of operational amplifiers here allows for proof of concept in this design.

The basis for the design of the band pass filters is taken from references 18, 21, and 22. The operational amplifiers employed to construct the filters are LM318 operational amplifiers [Ref. 6]. The second order band pass filters can be changed to fourth order by cascading a second identical stage. Appendix C contains the frequency response of the band pass filter designed at a center frequency of 76.2 kHz.

H. CODE DIVISION MULTIPLE ACCESS

Spread spectrum communications provide a degree of privacy. When the code for a particular user group is only distributed among authorized users, the

code division multiple access (CDMA) process provides communications privacy since the transmissions cannot easily be intercepted by unauthorized users without the code. The spread spectrum signals share the same frequency band, and there is a certain amount of crosstalk, or mutual interference. This interference does not make communications impossible, however, it degrades the performance of the system. The degradation in performance due to the multi-user interference is analyzed in the next chapter.

The DS/CDMA-BPSK system with four users was designed and built. The simplified system block diagram is given in Figure 20.

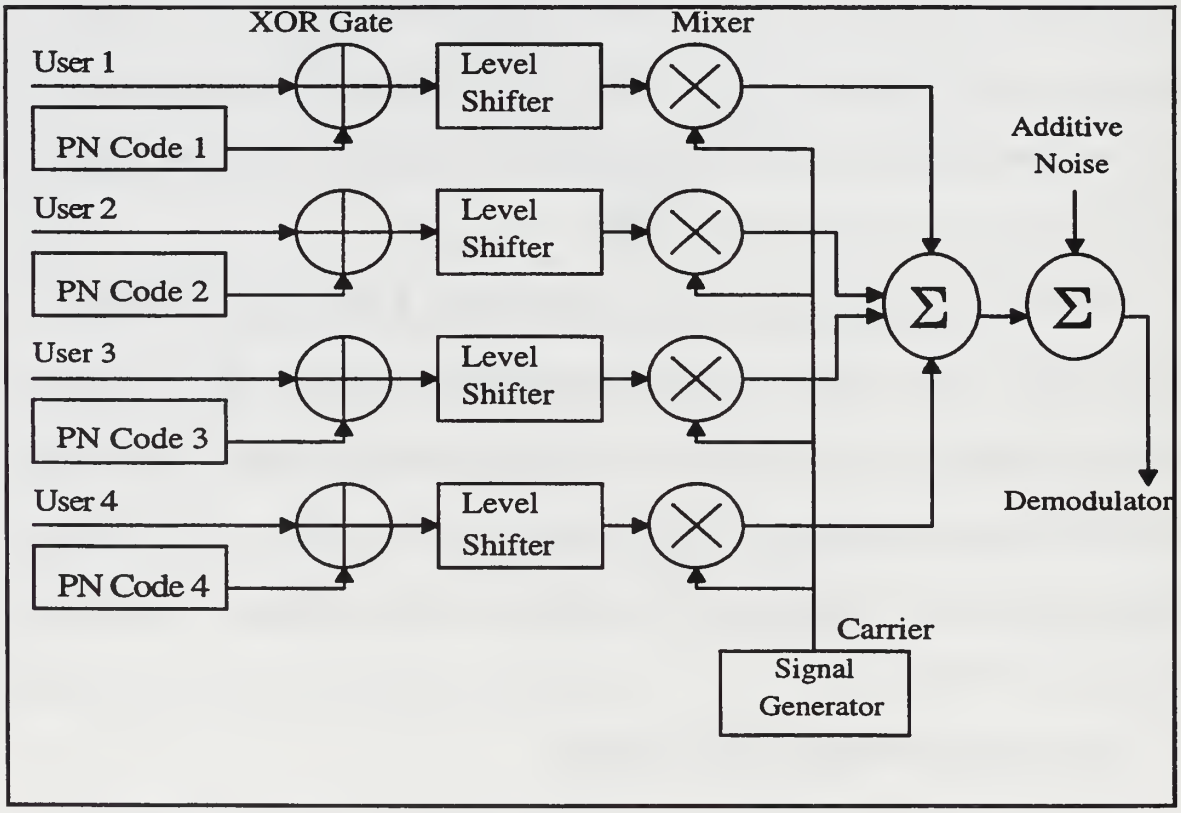

Figure 20. DS/CDMA-BPSK System with Four Users

For the multiple-user application, the information bits are spread by the Gold sequences, which are the most convenient sequences since they have the smallest cross-correlation values. The set of Gold sequences includes the two preferred-pair of m-sequences and modulo-2 sums of the first m-sequence and cyclic shifts of the second m-sequence. In particular, the set of four Gold sequences [Ref. 3] is

$$S(\text{Gold})=\{\underline{x}, \underline{y}, \underline{x} \oplus \underline{y}, \underline{x} \oplus T^{-1}\underline{y}\} \tag{2.3}$$

where $\underline{x}$ and $\underline{y}$ are the preferred pair, $\oplus$ is the modulo-2 sum operator, and T^{-1} is one bit shift left operator. The Gold sequences assigned for each user are derived from the different combinations of the preferred pair. The generations of the four PN codes are shown in Figure 21.

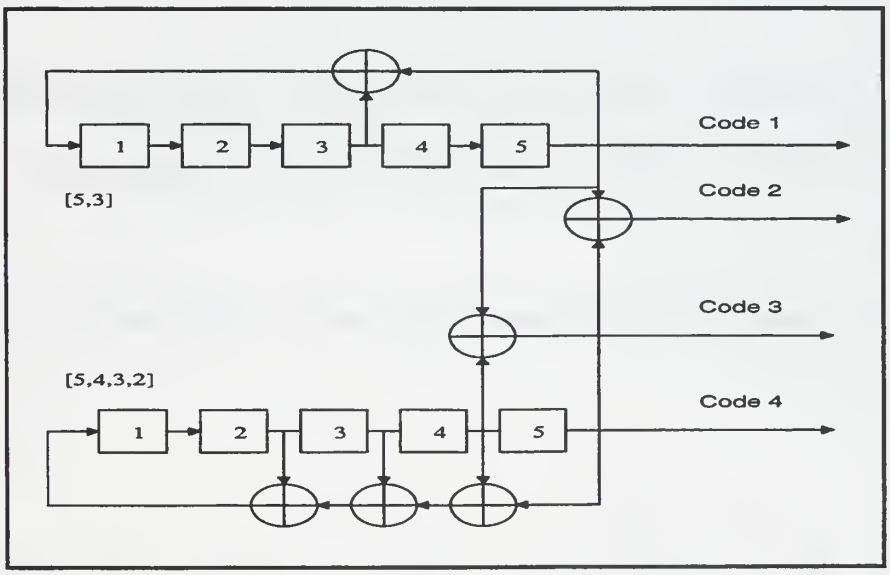

Figure 21. Gold Sequence Generator for the Preferred Pair [5,3] and [5,4,3,2]

The performance of a direct sequence CDMA system has been extensively analyzed in Ziemer and Lam [Ref. 2, 3]. For system design purposes, the Gaussian approximation is extensively used [Ref. 3]. In this model, the multi-user interference is treated as Gaussian noise with zero mean and variance determined by K and N where K is the number of CDMA users and N is the PN code length. This simplifies things greatly because a Gaussian random variable is completely characterized by its mean and variance. The standard Gaussian approximation for bit error probability for direct sequence CDMA BPSK is given by [Ref. 3]:

$$P_b \cong Q\left(\left[\frac{K-1}{3N}+\frac{N_0}{2E_b}\right]^{-1/2}\right) \tag{2.4}$$

where E_b is the average energy per bit, $N_0/2$ is the AWGN power spectral density, K is the number of CDMA users, N is the PN code length, and $Q(\cdot)$ is the Q-function.

A more accurate formula, the improved Gaussian approximation is given by [Ref. 25]:

$$P_b \cong \frac{2}{3}Q\left(\left[\frac{K-1}{3N}+\frac{N_0}{2E_b}\right]^{-1/2}\right)+\frac{1}{6}Q\left(\left[\frac{K-1}{3N}+\frac{\sqrt{3}c}{N^2}+\frac{N_0}{2E_b}\right]^{-1/2}\right)+\frac{1}{6}Q\left(\left[\frac{K-1}{3N}-\frac{\sqrt{3}c}{N^2}+\frac{N_0}{2E_b}\right]^{-1/2}\right)$$

(2.5)

where

$$c^2 = (K-1)\left[N^2\frac{23}{360} + N\left(\frac{1}{20}+\frac{K-2}{36}\right) - \frac{1}{20} - \frac{K-2}{36}\right] \tag{2.6}$$

In the next chapter, the P_b obtained with the improved Gaussian approximation (Eq. 2.5) is compared with the experimental measurements.

III. TEST RESULTS

The first performance test is conducted to measure the bit error rate of the BPSK system without the PN Code. After adjusting the carrier amplitude A to the value of 0.41 V, the energy per bit is computed from

$$E_b = PT_b = \frac{A^2 T_b}{2} \tag{3.1}$$

and found to be -41.4 dB where the bit duration (T_b) is equal to 833.33μsec.

Bit error rate (BER) during a given test is an indication of data quality:

$$BER = \frac{\text{the Number of Errors}}{\text{the Number of Received Bits}} \tag{3.2}$$

For example, if 12 errors occur during a 10000 ($1x10^4$) bit test, the BER is $\frac{12}{1x10^4}$ = 1.2 x 10^{-3} [Ref. 5]. When E_b is adjusted to -41.4dB, 7 errors are counted during 10000 bit test and the BER is recorded as $0.7x10^{-3}$.

To establish the bit energy-to-noise density ratio E_b/N_o, the noise power spectral density N_o is estimated at high BER, where the noise dominates the receiver performance. Since the exact signal power is known and the corresponding bit error rate is measured via BER equipment (HP1645A), the

noise density N_0 (W/Hz) can be approximated by using the ideal BER of BPSK at the signal-to-noise ratio which yields a BER of around 10^{-3}. The ideal BER of BPSK is

$$BER = Q\left(\sqrt{\frac{2E_b}{N_0}}\right) \tag{3.3}$$

Using this approach, we found the noise power spectral density N_o to be 1.45×10^{-5} W/Hz at E_b=-41.4dB, and this value is used to establish E_b/N_o for subsequent BER measurements. The theoretical and experimental BPSK bit error rate (BER) curves are plotted in Figure 21.

There is approximately 0.5 dB degradation in E_b/N_0 for the experimental BPSK at BER=3×10^{-5} and about 0.3 dB at BER$\leq 10^{-5}$.

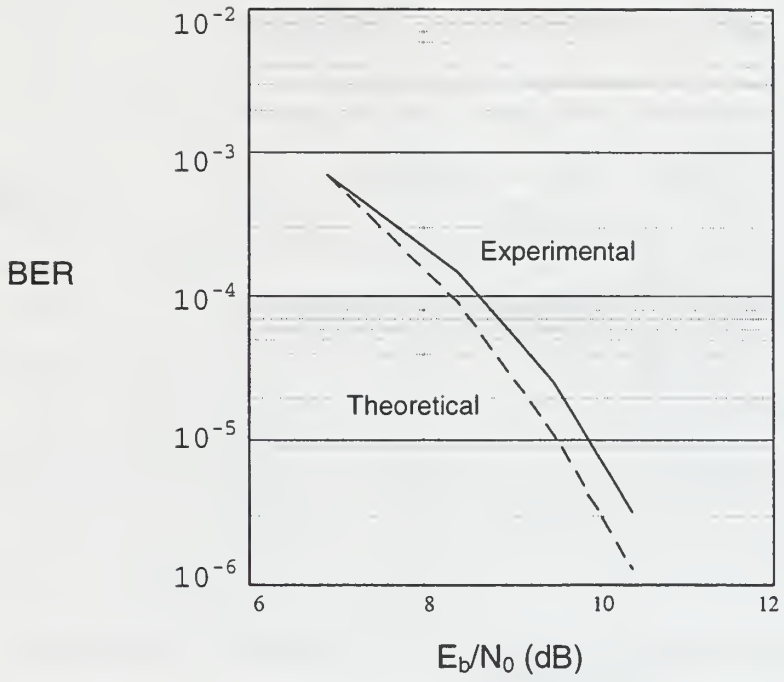

Figure 22. The Theoretical and Experimental BPSK Bit Error Rate Curves
(- - - Theoretical, ⎯ Experimental)

The following performance tests are conducted with the PN codes for K=1, 2, 3, and 4. All channels corresponding to each user are summed by a non-inverting adder (LM 741), and the same carrier power is applied to each mixer before the adder (Figure 20).

The information data and the received data are connected to the BER equipment (HP1645A Data Error Analyzer) [Ref. 5] so that errors could be counted digitally. Four sets of data were recorded (K=1, 2, 3, and 4). The BER values are shown in Table 3.1 for various E_b/N_0 and plotted in Figure 23.

	E_b / N_0 (dB)			
	6.9 (dB)	8.4 (dB)	9.5 (dB)	10.4 (dB)
BPSK (Experimental)	0.7×10^{-3}	1.5×10^{-5}	3×10^{-5}	3.2×10^{-6}
K=1	1.3×10^{-3}	1.8×10^{-4}	3.1×10^{-5}	4×10^{-6}
K=2	1.8×10^{-3}	4.1×10^{-4}	7.8×10^{-5}	2×10^{-5}
K=3	3.4×10^{-3}	1.1×10^{-3}	2.5×10^{-4}	7×10^{-5}
K=4	5.1×10^{-3}	2.3×10^{-3}	7×10^{-4}	3.4×10^{-4}

Table 3.1. Experimental Bit Error Rates of DS-CDMA/BPSK System for K=1,2,3,4.

The Gaussian approximation for K=2, 3, and 4 using Equation 2.5 is also shown in Figure 23.

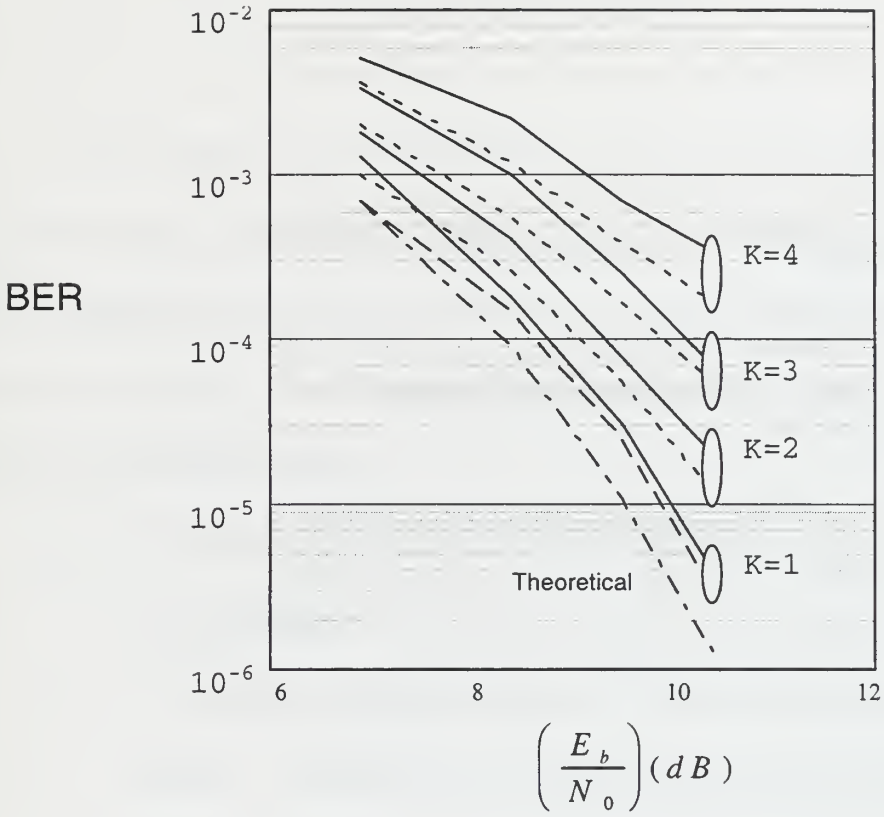

Figure 23. Theoretical and Experimental Bit Error Rate Curves for DS-CDMA/BPSK System.
(CDMA: - - - - Theoretical, ——— Experimental,
BPSK: - · — · — Theoretical, — — — Experimental.)

The theoretical BER curves for K=2, 3, and 4 are plotted using the improved Gaussian approximation formula (Eq. 2.5) [Ref. 3, 25]. From Figure 23 it can be observed that at BER=10^{-3} there is a degradation in E_b/N_0 of about 0.5 dB for the experimental DS-CDMA/BPSK system. At BER=10^{-4}, the degradation is about 0.2 dB for K=2, and 3. In summary, the experimental results agree well with the improved Gaussian approximation taking into account other imperfections such as filtering in the demodulator.

IV. CONCLUSIONS

In this thesis, a DS-CDMA/BPSK spread spectrum modem is designed and its multi-user performance is tested for up to four users. The bit error rate curves showing the multi-user performance of the modem are very close to the theoretical results. The following points are recommended to obtain more precise and practical results:

1. The laboratory tests should be made by using a more accurate bit error analyzer.
2. This design can be modified for higher data rates and processing gains. However, this will require high speed components with lower tolerances.
3. The design described here contains some additional equipment, such as carrier and clock generators, which are impractical for a final design. These signal generators can be replaced by a module producing the required wave forms through a crystal oscillator and division chains.
4. This preliminary hardware design is power inefficient by today's standards. It is significant to note that in many cases in this design the TTL components used are of the least power efficient variety and were chosen based on availability alone. Several modification

to the existing design can be implemented. Power savings can be achieved by converting all 7400 series components to their 74LS00 equivalent components.

5. For greater stability, it is recommended that the signal generators (MODEL 142HF) be replaced with the crystal oscillators or with the sine-wave generators (AD630). The signal generators were initially selected because they could be adjusted over a wide range of frequencies which allowed for design changes. The crystal oscillators allow for only slight frequency adjustments.

6. The early minus late module can be modified by eliminating one-half of the two branches employed. This can be done if both early and late branches are switched alternately through the remaining half and then adding a sample-and-hold to retain these signal values for subsequent subtraction. This would result in a better balance between early and late signals, since they are generated from the same path.

These points are not important as far as the functionality of the design is concerned. This preliminary design, as it is intended, provides a basic solution to the final realization. Substantial power savings can be achieved but, for this design, the importance lies in the realization of a functional prototype and to this end the design is a success.

APPENDIX A

FUNCTIONAL BLOCK DIAGRAMS

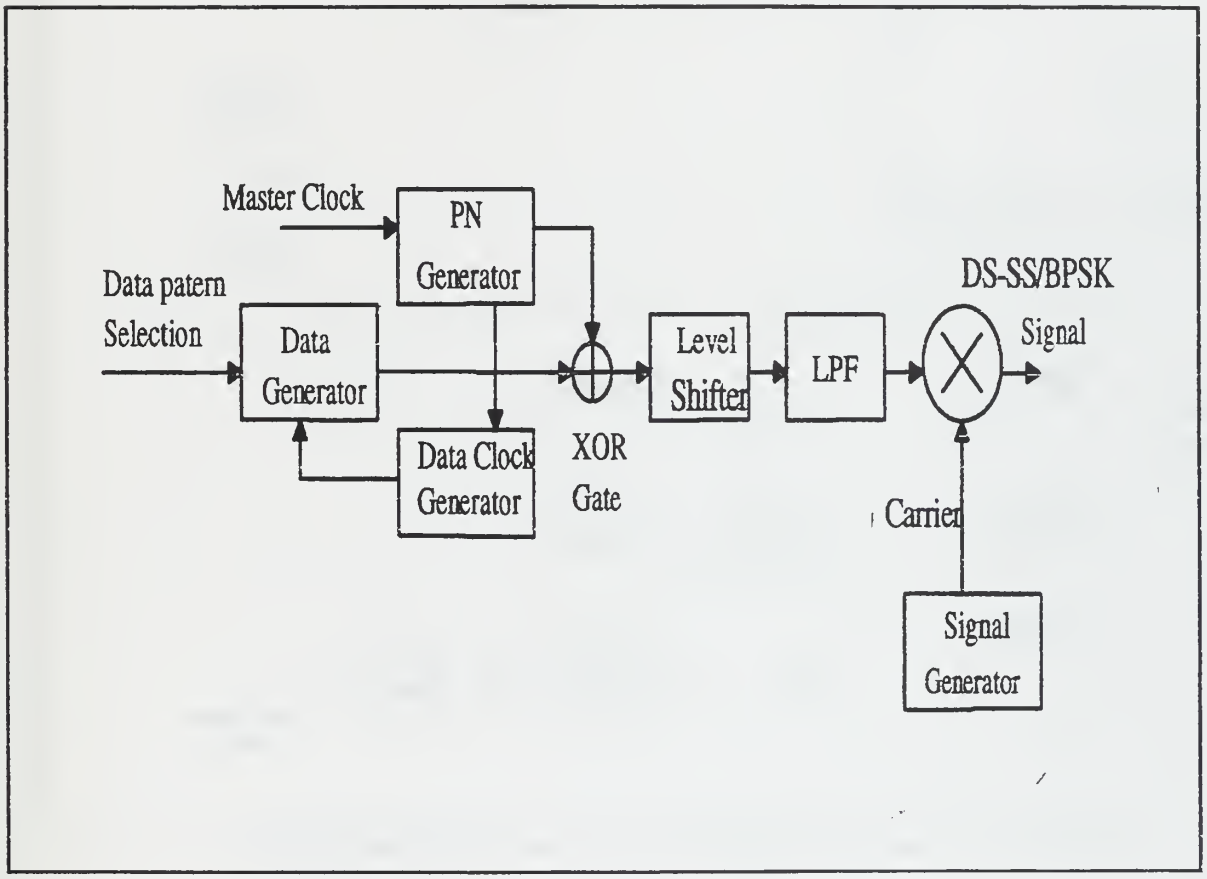

Figure A.1. The Modulator Functional Block Diagram.

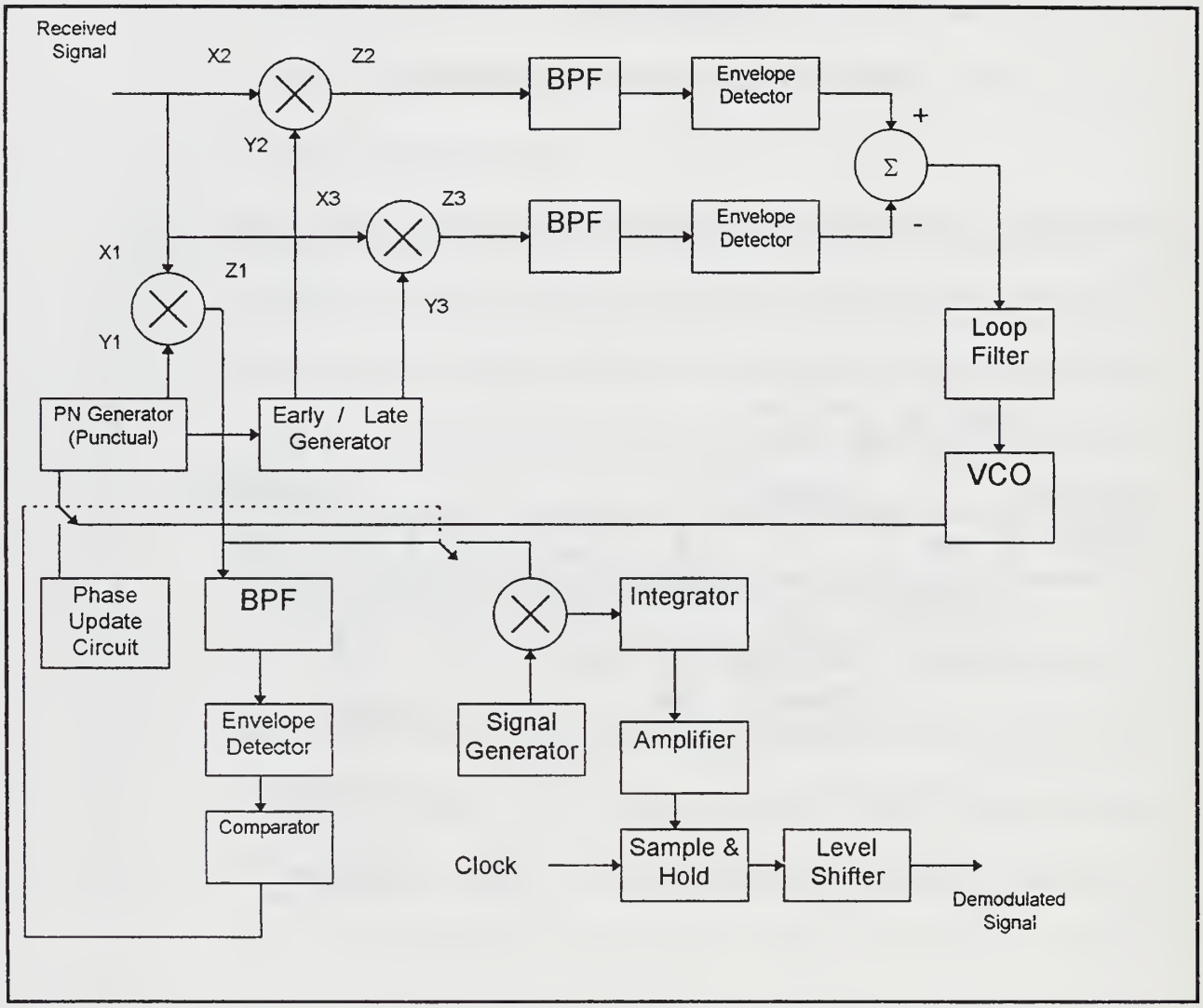

Figure A.2. The Functional Block Diagram of the Demodulator.

APPENDIX B

CIRCUIT SCHEMATICS

Figure B.1 Modulator

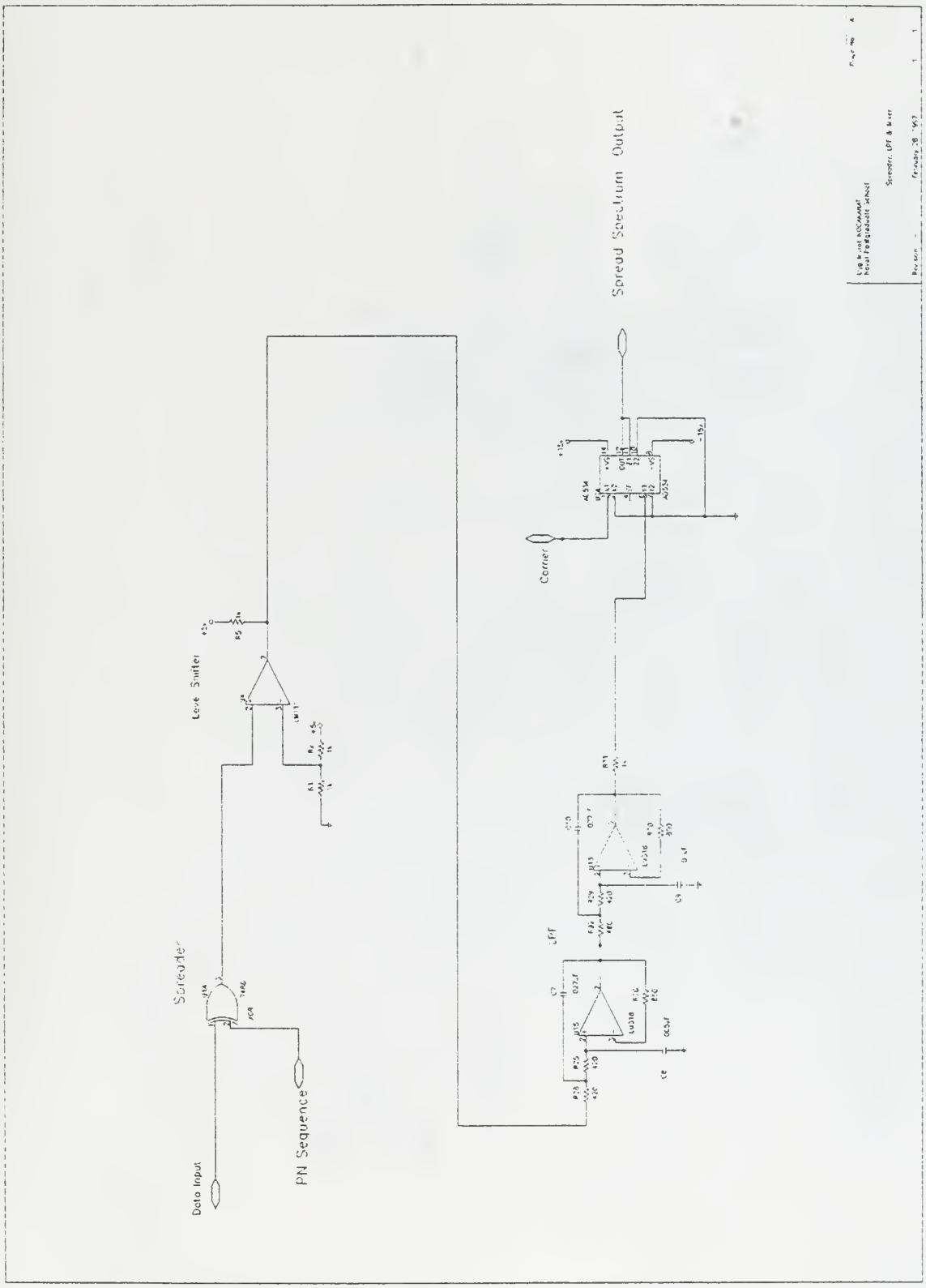

Figure B.2 Spreader , LPF, and mixer

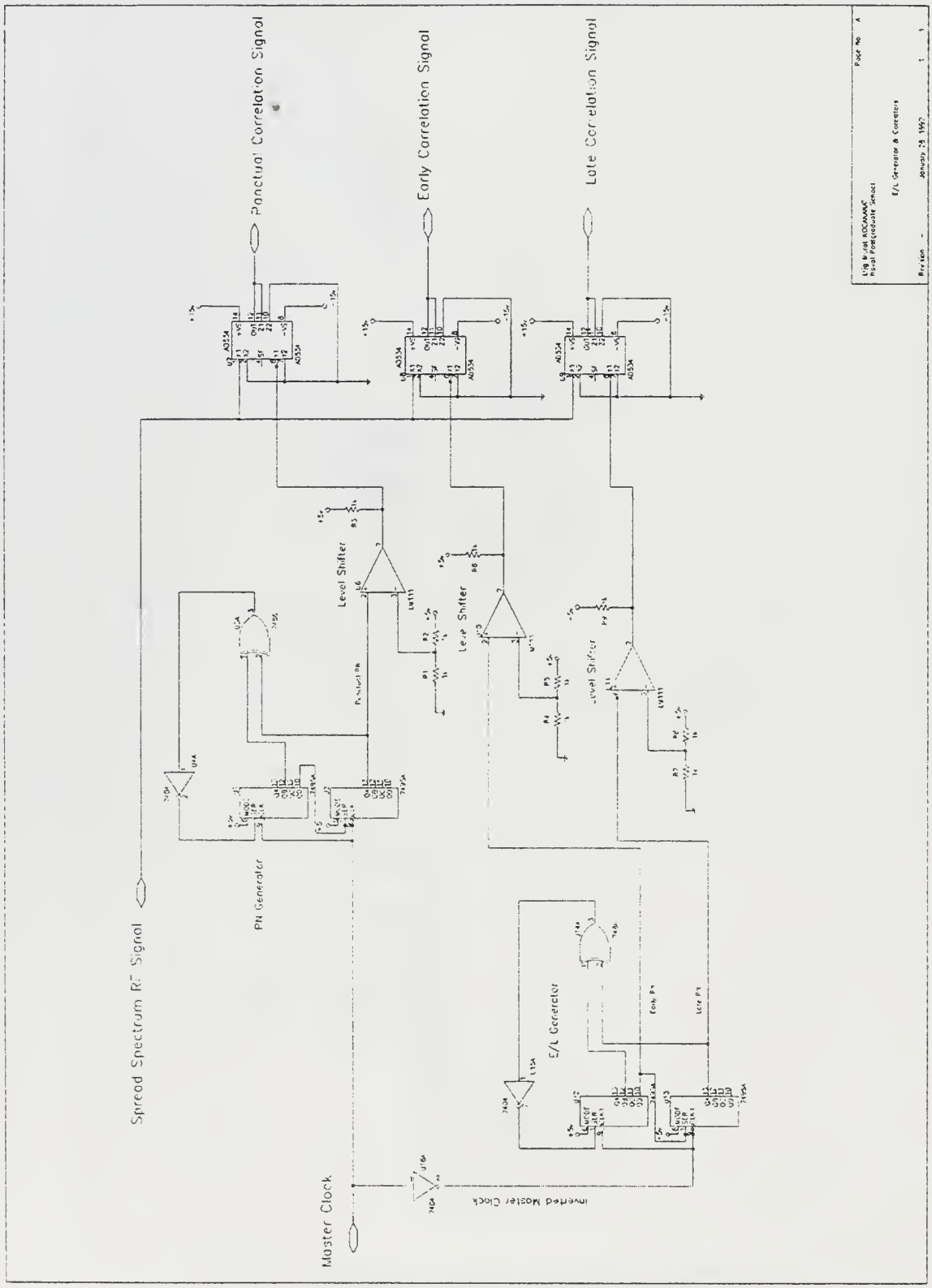

Figure B.3 Early / Late generator and correlators

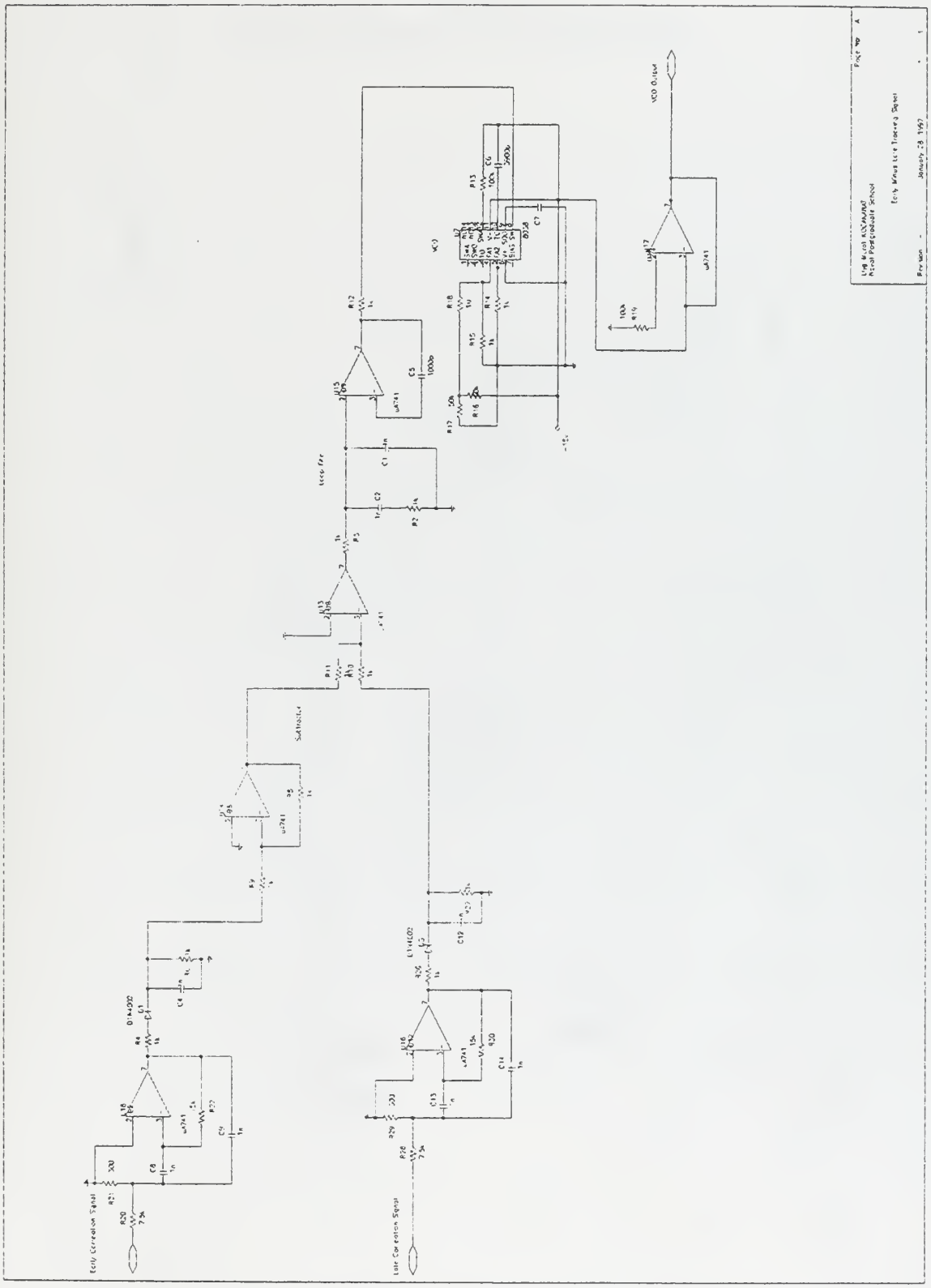

Figure B.4 Early minus Late tracking signal

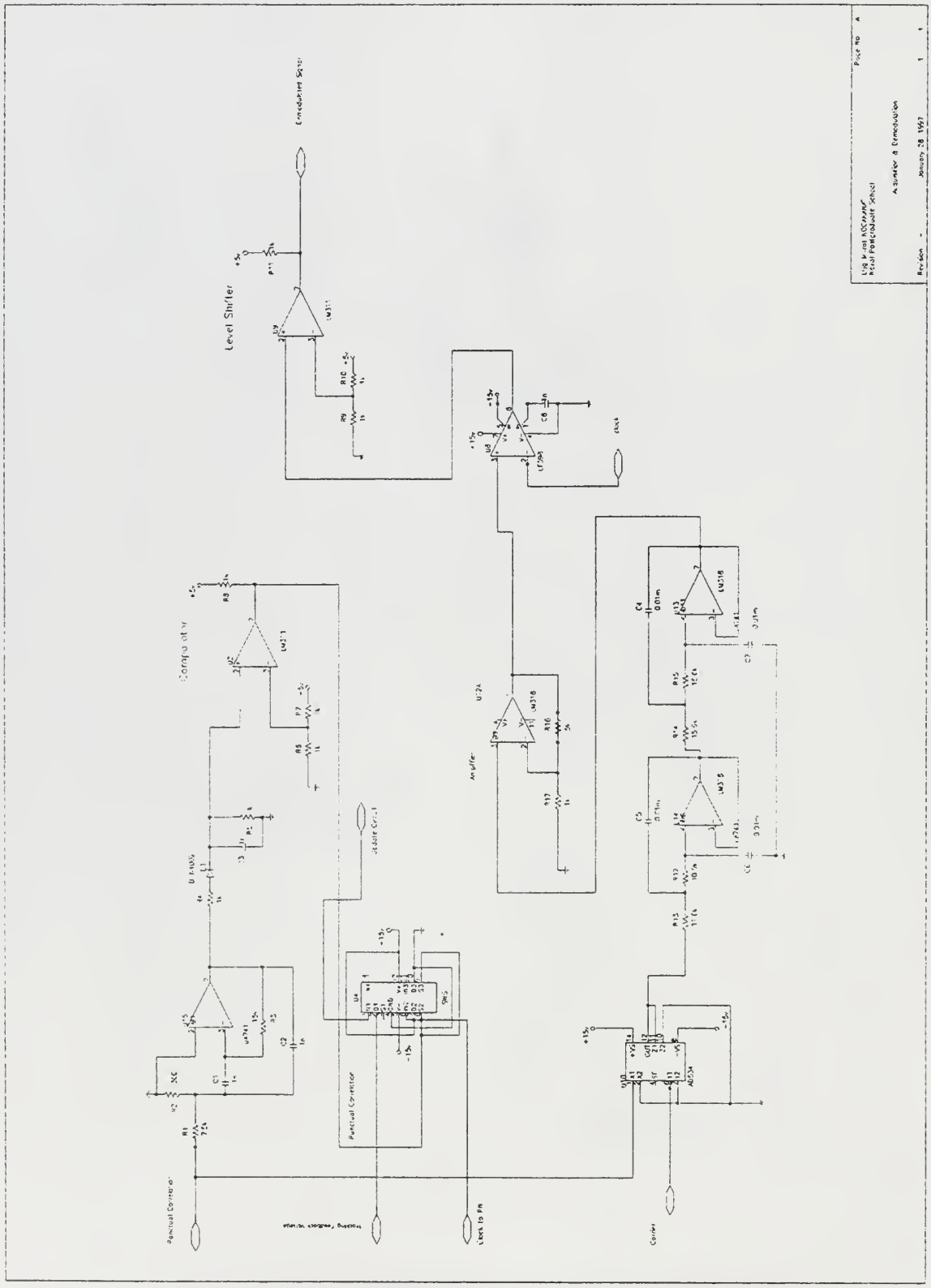

Figure B.5 Acquisition and demodulator

APPENDIX C

BAND PASS FILTER CONSTRUCTION

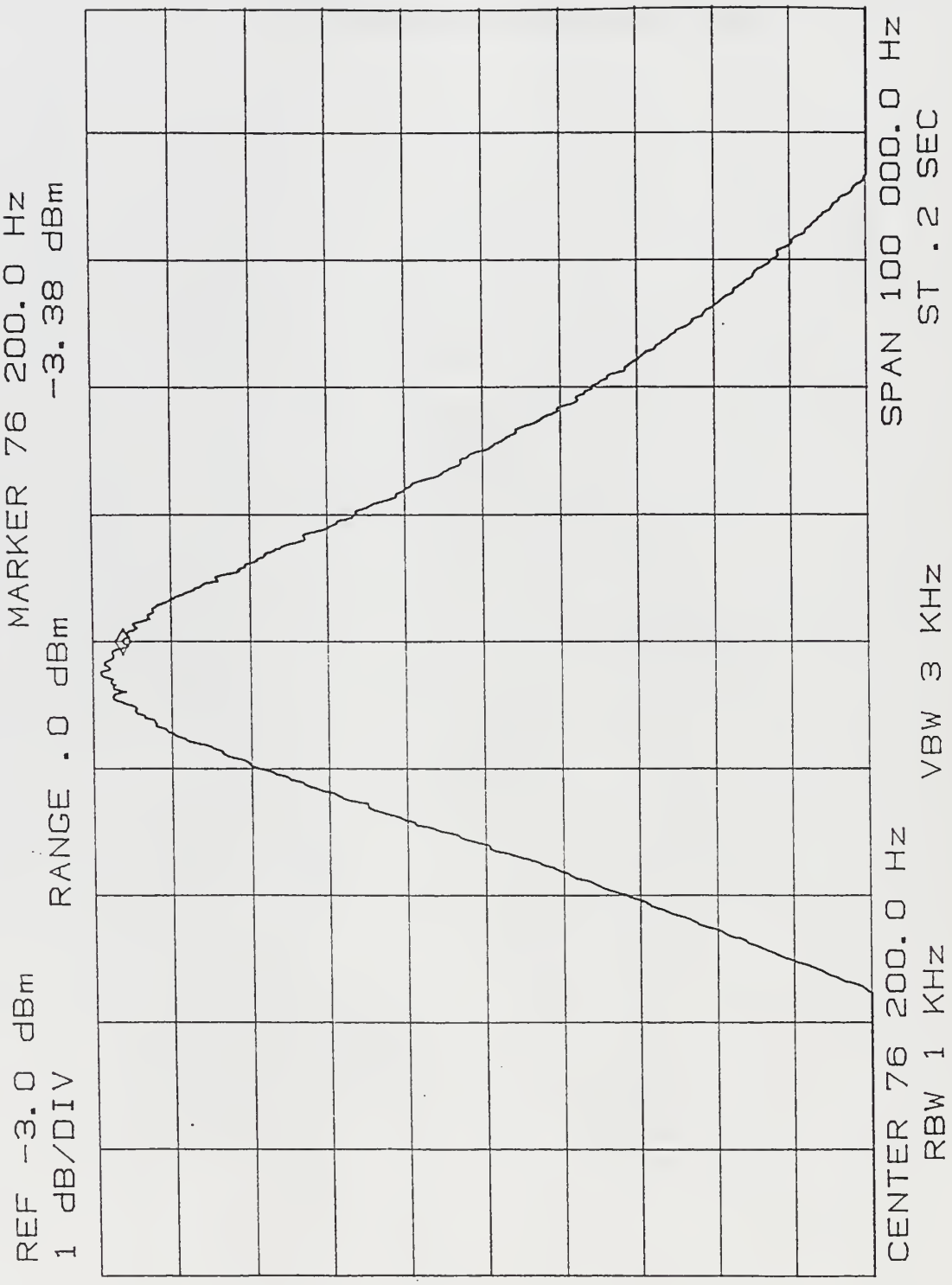

Figure C.1 Frequency response of the BPF with f_c=76.2 kHz.

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